5) - Metalization: used to create contact with Silicon and to make inter connections on chip.

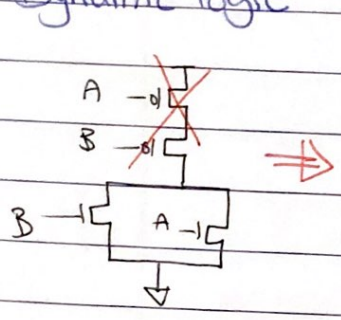
- Assembly and packaging:
the chips on the wafer are seperated and packaged by a method (Scribing and cleaving)

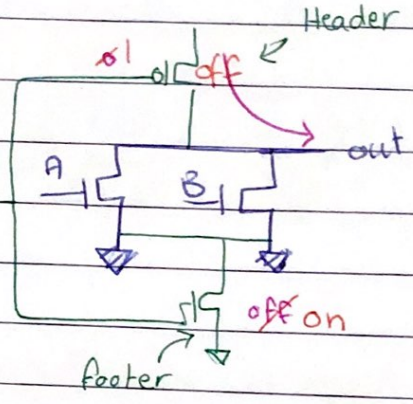
- Main IC charactaristics:
  - Power
  - Area
  - speed
  - timing

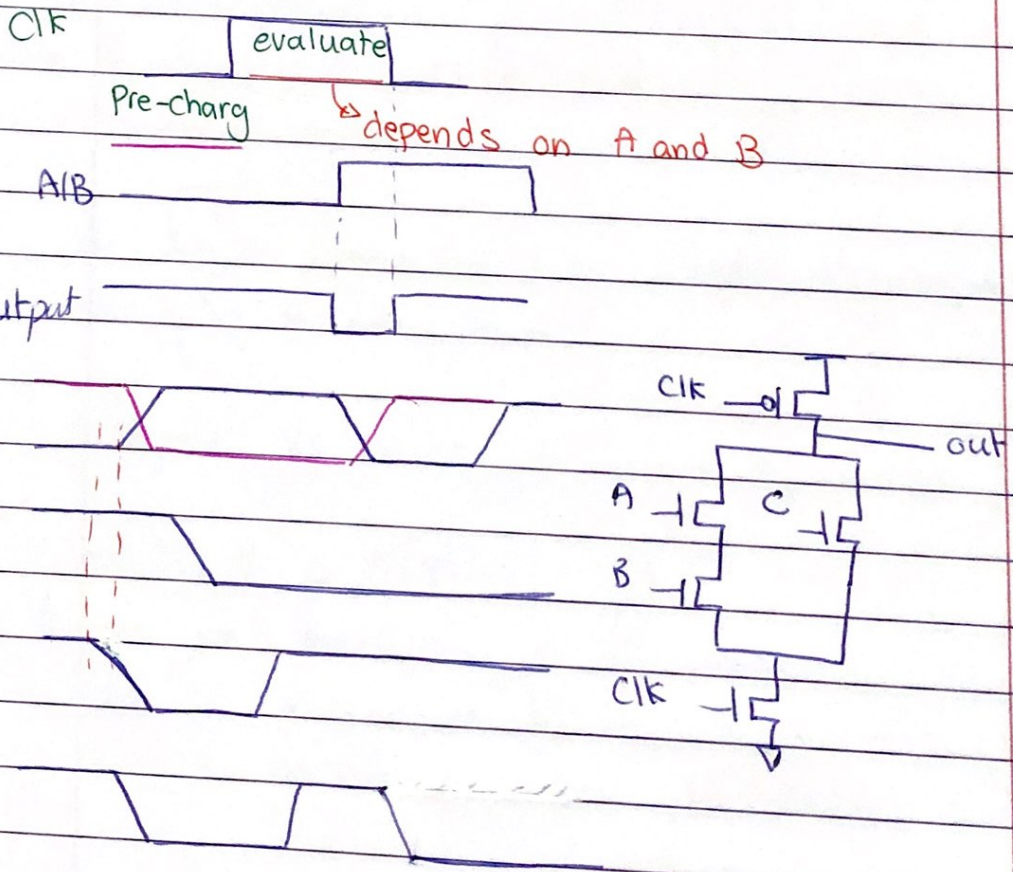
lect:10 nMOS Logic gates

- دايما الـ nMOS هي اللي بتشتغل الشغل و دايما b
  . min size pdevice و minimum size pdevice

Dynamic logic

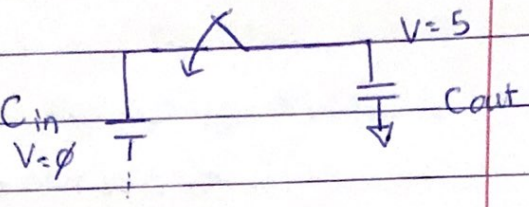






- Charge sharing

$Q_f = Q_{in} + Q_{out}$



$V_f(C_{in} + C_{out}) = C_{in}\phi + C_o(5)$

$$V_f = \frac{C_{out}(5)}{C_{in} + C_{out}}$$

full keeper

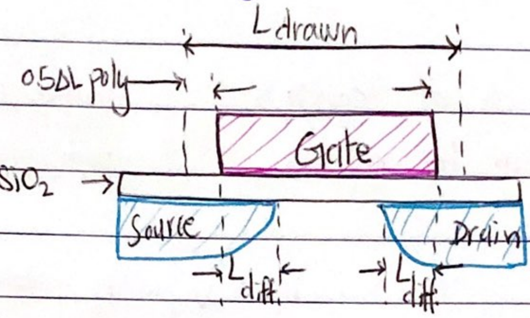
Full keeper is used to prevent the change in the output

to prevent this.

- Sequential logic

notes: cont...

Le – the effective channel length



صراحة بعرفش
مين عاملة
واذا معكوس
أو لا.

$L_e = L_{drawn} - \Delta L_{poly} - 2L_{diff}$

– For CMOS, as the channel length decreases, V_t will also decrease.

The depletion region below the gate can no longer be approximated a rectangular region

– As Vd is higher, the drain depletion region increases causing a decrease in V_t.

– A higher V_T leads to lower ~~V_d~~ device current

– mobility $\mu \Rightarrow \mu(T) = \mu_0\left(\frac{T}{T_0}\right)^{-3/2}$

↳ as ~~on~~ T increases μ decreases

as T increases V_t increases

as T increases Ids decreases

nMOS:

on: $V_{in} > V_t$

off: $V_{in} < V_t$

Sour

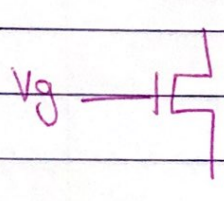
↳ Source is at lowest potential for nMOS

pMOS:

on: $V_{in} < V_{DD} - |V_t|$

off: $V_{in} > V_{DD} - |V_t|$

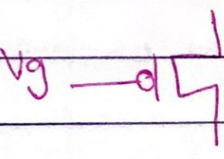
Source on highest potential for pMOS



$V_g > V_i + V_t \Rightarrow V_o = V_i$

else

$V_g < V_i + V_t \Rightarrow V_o = V_g - V_t$



$V_g < V_i - |V_t| \Rightarrow V_o = V_i$

else

$V_g > V_i - |V_t| \Rightarrow V_o = V_g + |V_t|$

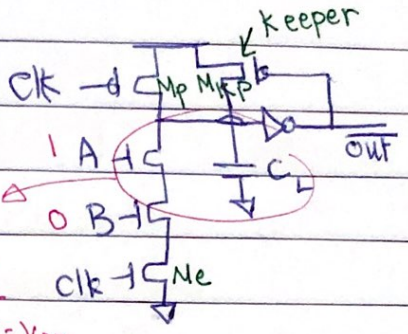
Source is the ~~boost~~ lowest potential for nMOS and the highest potential for pMOS

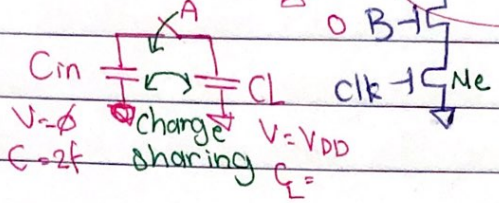
$m_1 \rightarrow$ highest resistance

$m_6 \rightarrow$ lowest resistance

Ch 10: cont...

solution to charge leakage



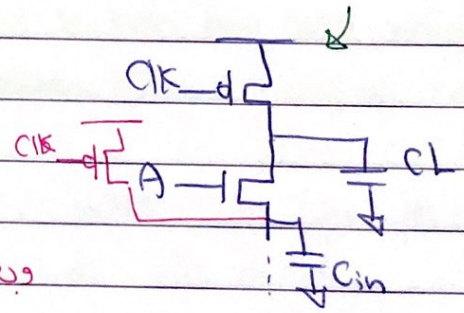


$Q_f = Q_{int} + Q_L$

$(C_{in} + C_f) V_f = C_{in} V_{in} + C_L V_{dd}$ ✱ $Clk_L = 0$

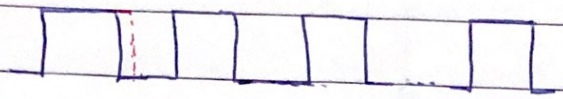
$V_f = \frac{C_L}{C_{in} + C_L}$

هاد جزء من الرسمة موجود



عشان أحل مشكلة لو ال Clk اجت 0 و ال A 1 مع بعض وبصير بدي اشحن Cin و CL بضيف الجزء الزهري . اللي هو بشحن Cin

- Latch



delay in

- we have clk skew and clk jetter. ↓ clk

clk skew is due to wiring delay

clk jetter is due to the clk generator problems

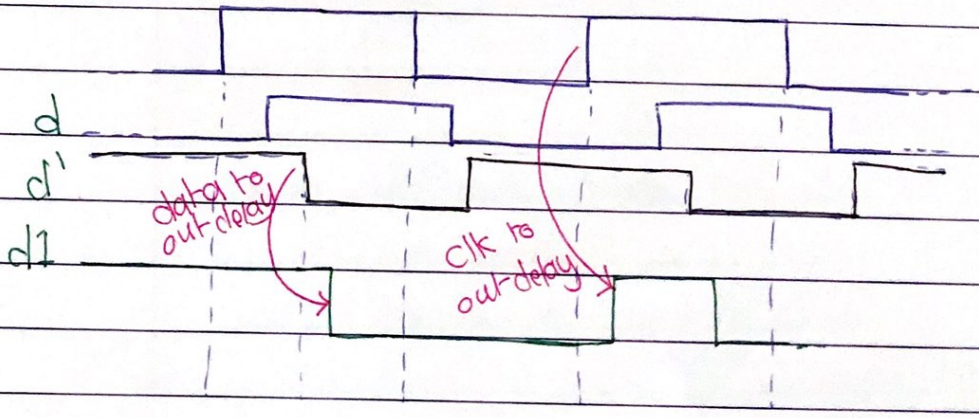
setup time: when we need the data to be ready to table it

holdup time: we need to hold the data ~~until the clk arrives~~ when changing the clk

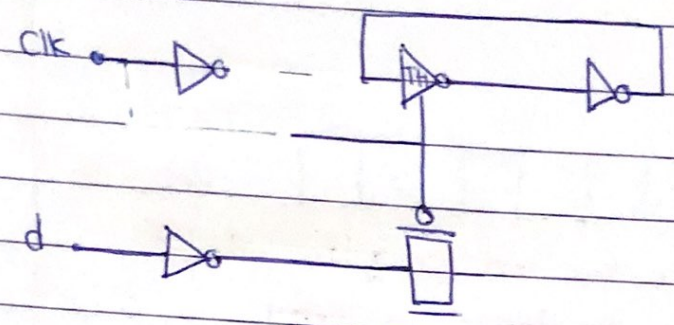
يعني فرضاً لـ nMOS ، لما الـ clk = 1 يكون الـ setup

و لما الـ clk = 0 يكون الـ hold up

(clk to out delay / data to out delay)



للرسمة ورا



الانفيرتر هستان عشان Passgate وبتأثر على الـ input
فالـ inverter بينهما ولو غير الـ load بتأثرش

Lect 11:

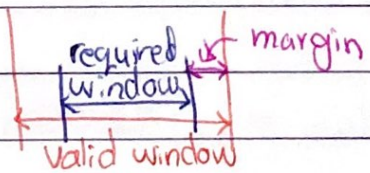
PLL generates the clock (analog)

⇒ we use clock buffer

we use FTRC model to model the wires  $(\rho, w, L, S..)$

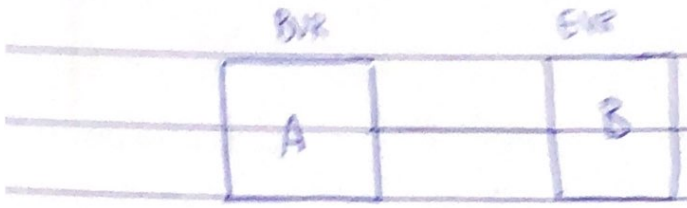
- Lead edge signal
  اللي هي الـ edge اللي بتاخد
  الـ active بتعتبر الـ signal
  الـ Trail بتكون العكس.

- timing window
  - Valid window ⇒ مدى الـ signal اللي بين ايها
    يقدر آخدها
  - required window ⇒ مدى انا بحتاج الـ signal تبقى
    تكون جاهزة

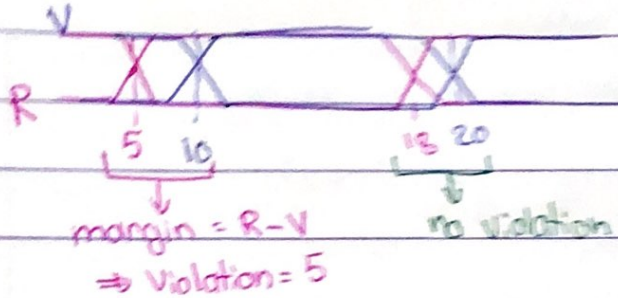


- margin: difference between the valid and the required window, it could be Positive or negative
  ↳ margin violation

bone of diversion → reference clock.



V R



- Required window ⇒ use br, bf
- Valid window ⇒ use ar, af

- 2 types of delay in latches → input
  → clock
- 1 type of delay in Flip-flop → clock

~~Margin~~

- Transparence window only happens in the latch

$$\text{Margin}(F_1 \to F_2) = T_{cycle} - clk \to Q_{FF_1} - T_{d_1} - (\text{MaxSkew}_{ck_1} + \text{Jitter}) - \text{setup}_2$$

$$= 0.25 - 0.023 - 0.185 - (0.015 + 0.016)$$

$$= 0.458 - (0.031)$$

$$= 0.427$$

$$\text{Margin}(F_2 \to F_3) = T_{cycle} - clk \to Q_{FF_2} - T_{d_2} - \text{setup}_3 - (\text{MaxSkew}_{ck_2} + \text{Jitter})$$

$$= 0.25 - 0.025 - 0.155 - (0.015 + 0.016)$$

$$= 0.057$$

---

* Power

- Electro Migration (EM)
- Self Heat (SH)

EM: when electrons move in wires in a spesific direction, it will destroy the wire by the time.

SH: when electrons move in wires in both directions, it will destroy the wire by self heat.

we should elemenate having a short circuit in static designs (guarentee that the devices wont be on at the same time)

⇒ we cant guarentee not having a short circuit in dinamic designs)